IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BOARD OF PATENT APPEALS AND INTERFERENCES

#17
LDS
2-21-03

Applicant:	Brian DONOVAN	Group Art Unit:	2155
Serial Nº:	09/410,202	Examiner:	David Y. Eng
Filed:	September 30, 1999		
Title:	ZERO OVERHEAD COMPUTER INTERRUPTS WITH TASK SWITCHING		

APPELLANT'S REPLY BRIEF UNDER C.F.R. §1.193(B)(1)

1600 ODS Tower
601 SW. Second Avenue
Portland, Oregon 97204-3157

February 10, 2003

Noted
DE
2/24/03

Commissioner of Patents
Box AF
Washington, D.C. 20231

Dear Sir:

Claims 2, 4 through 7 and 14 through 16 were rejected as unpatentable under 35 U.S.C. §103(a) as being unpatentable over the Madnick textbook.

Claim 4 calls for a microprocessor based computing system that includes a combination of devices and circuit elements. The preamble of claim 4 states that tasks are represented by task register sets and the system further includes peripheral devices that issue interrupt commands. Within this environment, there are three elements to the system. There is a task enable circuit that determines from predetermined inputs whether a task is ready for execution, a task priority selection circuit that is coupled to the output of

the task enable circuit and determines an order for the running of tasks and a task switching circuit coupled to an output of the task priority selection circuit for controlling the execution of tasks in a specified sequence.

According to the Examiner, Madnick shows these elements in various figures of the Madnick reference. For example, the "register sets" of the preamble are said to be "inherent" in the various blocks that are shown in FIG. 4-1. The problem with the drawing of 4-1 is that it is not an electronic circuit. Moreover, the "state model" described in section 4-1 is a process which is conducted largely by humans. For example, section 4-1 states

> "An operator took my code and caused it to be read into the computer and copied onto a disk where a job scheduler could examine it (hold state). Eventually, the job scheduler chose me to run and set up a process for me (ready state). To get my process into a ready state faster on a manually scheduled system [emphasis added], my friendly programmer might have inserted a green card (a $5 bill) in front of my deck."

This is obviously a description of the rules for running a computing center where tasks are represented by stacks of punched cards which are loaded into a data-processing machine manually. There is no circuit or electronic network having circuit elements in this reference which performs these functions automatically.

The subelements (a), (b) and (c) call for specific connections between the three circuits defined in claim 4. For example, the task priority selection circuit is coupled to an output of the task enable circuit. The Examiner alleges that these types of connections are shown in Madnick and refers to page 212. However, once again, there is no circuit shown at page 212. The Examiner's reliance on section 4-2 on page 215 is likewise misplaced. That paragraph states in part "In a time-sharing system ... the job scheduling policy may consist of admitting the first thirty users that log in (*i.e.*, arrive)." This is a description of

the activity of human beings. In this paragraph, the function of job scheduling is referred to as a "policy." This paragraph describes policies and procedures used in the computing center to allocate system resources. There is no description of a circuit for doing this.

The Examiner admits, however, that Madnick does not show an integrated circuit as called for in claim 2. The Examiner then performs an extraordinary leap of logic with the bold statement that "one of ordinary skill in the art should readily realize that the schedulers of Madnick can be executed by a microprocessor." This is an astounding conclusion without any evidentiary basis whatsoever. No art has been cited that shows computer circuits in a data processing system coupled together in the manner defined by the claims performing the functions defined by the claims. Madnick was published in 1974, long before the advent of the modern computer. While crude microprocessors may have existed in 1974, there is no showing in the prior art that the functions defined by the claims were implemented in circuitry in a microprocessor based computing system.

In section 4-2.2, "Policies," the nature of the system generally described in Madnick is revealed to be a computer operations center run by human beings. That section states "In a small computing center, this function may be done by an operator. He may choose arbitrarily, choose his friends, or choose the shortest job." The paragraph further states that in larger computing systems, the jobs are stored on a "secondary storage device" where the "job scheduler" can examine all such jobs. It is clear that the "job scheduler" is a human being. At best, there is software that performs some of this function. (At the top of page 216, there is a reference to "a particular scheduler" which makes reference to "the code.") In all of this discussion, however, there is no mention of hard-wired circuitry that actually performs the functions required of the circuits that are set forth in claim 4.

Claim 2 is similar but the claim is a method claim. Like claim 4 however, it is the

integrated circuit that performs the steps of the method. The Examiner has cited no prior art which shows an integrated circuit operating in a computer system having input sources that issue interrupt signals and that performs the functions of assigning a priority level for each task, changing the priority level as a function of time, and beginning the execution of a first task when the priority level of the first task exceeds the priority level of all other tasks. Madnick does not show any integrated circuit performing these functions in a computer system that has input sources issuing interrupt signals for requesting the performance of a task. Instead, the Examiner has assumed that, based upon Madnick, it would have been obvious to provide these functions in an integrated circuit. No evidence in support of this proposition has been cited.

The Examiner's rejection of the claims on the grounds of obviousness are based upon the faulty premises that Madnick either actually shows circuitry for carrying out the functions recited in the claims, or, if such is not the case, one of ordinary skill in the art could have developed circuits to carry out the functions described in Madnick. As a final argument, the Examiner states that the claims are "means plus function" claims, a position which is not supported by the record. The claims are not couched in means plus function format. The fact that no counters, registers, or other circuit subcomponents are recited in the claims does not transform the electronic circuit that is recited in the claims into simply a statement of means plus function.

The Examiner has been unable to find prior art implementing the claimed network performing these functions in the twenty-three years following the Madnick reference. T the only conclusion that can be drawn from this lack of evidence is that there was a long-felt need in the art and that others had failed to put the combination together. This is a secondary consideration of nonobviousness, which must be considered in any obviousness

analysis. For the Examiner to conclude, then, that this circuit would have been obvious to one of ordinary skill in the art twenty-three years after the publication of the Madnick reference with no references to support his conclusion flies directly in the face of the historical evidence which shows that, in fact, it was never done prior to this invention.

Respectfully submitted,

William O. Geny

CERTIFICATE OF MAILING

I hereby certify that this *APPLICANT'S REPLY BRIEF UNDER C.F.R. §1.193(B)(1)* is being deposited with the United States Postal Service as first class mail on February 10, 2003 in an envelope addressed to: Commissioner for Patents, Box AF, Washington, D.C. 20231.

Dated: February 10, 2003

William O. Geny

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CORRECTED APPENDIX TO APPEAL BRIEF ON BEHALF OF APPLICANT

Claims

1. Cancelled by amendment of October 2, 2002.

2. A method for ordering the performance of tasks in a computer system, said computer system having input sources that issue interrupt signals for requesting the performance of a task, said method comprising:

(a) providing an integrated circuit having circuit components for automating the selection of tasks to be performed by said computer system;

(b) wherein the integrated circuit performs the following steps:

(i) assigning a priority level for each task based upon a selected parameter of an interrupt signal;

(ii) changing each priority level as a function of time; and

(iii) beginning the execution of a first task when said priority level of said first task exceeds said priority level of all other tasks.

3. Cancelled by amendment of October 2, 2002.

4. In a microprocessor-based computing system having a CPU for executing tasks represented by task register sets and further including peripheral devices that issue interrupt commands, an interrupt and task change processing circuit comprising:

(a) a task enable circuit for determining from predetermined inputs whether a predetermined task is ready for execution by the central processing unit,

(b) a task priority selection circuit coupled to an output of the task enable circuit for determining an order for the running of tasks that have been determined ready for execution by the task enable circuit; and

(c) a task switching circuit coupled to an output of the task priority selection circuit for controlling the execution of tasks in a sequence determined by the task priority selection circuit.

5. The interrupt and task change processing circuit of claim 4 wherein said task priority selection circuit includes a variable rate task priority incrementing circuit for varying an assigned priority of a task such that said priority increases with time, whereby its execution is caused to occur within a predetermined period of time.

6. The interrupt and task change processing circuit of claim 4 wherein the task enable circuit includes a task linking circuit for linking together groups of tasks which are dependent upon each other.

7. The interrupt and task change processing circuit of claim 4 wherein the task enable circuit is responsive to a task interrupt signal for designating a task as ready to run, said task enable circuit including a timer for generating said task interrupt signal after a predetermined period of time.

8. The interrupt and task change processing circuit of claim 4 further including a trace enable circuit for recording register states of selected registers during a preselected clock cycle.

9. The interrupt and task change processing circuit of claim 4 wherein the task switching circuit is coupled to a zero overhead multiplexing circuit for storing a later task in a first set of latches during a first clock cycle while simultaneously switching a previously stored earlier task stored in a second set of latches into a task switch controller during the same clock cycle.

10. In a microprocessor-based computing system having a CPU for executing tasks represented by task register sets and further including peripheral devices that issue interrupt commands, the combination comprising:

(a) an interrupt and task change processing circuit for responding to interrupt commands and for placing tasks in an order of priority for execution by the CPU, and

(b) a zero overhead multiplexing circuit coupled to the interrupt and task change processing circuit for storing a later task in a first set of latches during a first clock cycle while simultaneously switching a previously stored earlier task stored in a second set of latches into a memory unit during the same clock cycle.

11. The combination of claim 10 wherein the interrupt and task change processing circuit includes a task enable circuit for placing a task in a status in which it is ready for execution by the CPU.

12. The combination of claim 11 wherein the interrupt and task change processing circuit includes a task priority selection circuit for assigning a task priority to tasks which are ready for execution by the CPU.

13. The combination of claim 12 wherein the interrupt and task change processing circuit includes a task switching circuit for loading tasks ready for execution by the CPU into said zero overhead multiplexing circuit based upon their task priority.

14. The method of claim 2 wherein step (b)(ii) is accomplished at different rates of time for different tasks.

15. The circuit of claim 4 wherein said task priority selection circuit includes means for assigning a priority level for each task and timing means for changing said priority levels as a function of time.

16. The circuit of claim 15 wherein said timing means includes means for varying the rate of change of said priority levels as a function of time.

CERTIFICATE OF MAILING

I hereby certify that this *CORRECTED APPENDIX TO APPEAL BRIEF ON BEHALF OF APPLICANT* is being deposited with the United States Postal Service as first class mail on February 10, 2003 in an envelope addressed to: Commissioner for Patents, Box AF, Washington, D.C. 20231.

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William O. Geny